88.9mm (3.5") (3.1")

78.8mm

AXIS TEN PRODUCTS

Frequency to Voltage Converter ~ ATP2/2 FEC Order Number ~ 179932

General Description This product is a versatile Frequency-to-Voltage converter and Tachometer. It finds applications in many industries 63.5mm (2.5") ranging from Automobile R&D to Ship building and Mining. It is used in anything from closed-loop servo control to 53.3mm (2.1" simple monitoring and display systems. Conveyor or drive shaft speed control and monitoring are typical industrial applications. To enable trouble-free and rapid commissioning, popular signal sources and their recommended connection scenarios are shown as circuit diagrams over-leaf. The circuit is specified to work at frequencies up to AXIS TEN PRODUCTS PSU=+9V TO +24V 70kHz, and needs just two capacitors selecting or inserting to make it work. (+26V ABS MAX) F/V TACHO/SERVO (+60V LOAD DUMP) VERSION: ATP2/2 (Continued over leaf.) IC2 0000 **o**]/ 80 00 +PSU **O** – R18 O R20 R21 R21 R23 Top two Terminals are Power in, V_(PSU) = +9V to +24V dc (+26V Abs. Max.) at <20mA plus Detector 0 supply current. Circuit can with-stand +60V transients (load dumping) from poorly regulated supplies. C9 0 3 0000 0 ADJUST +DET C8 FULL 0 - R13 - O SCALE 00 0 0 AUX C6 0 Ο Central eight Terminals are Signal in. The most common Signal sources are listed below: o⊣ ⊢o -0 R6 **O** R19 0 R3 Б 0 PNP Ο FILTER (2) ò Hybrid Sensors - open collector PNP output Ó ÓÓ Ó ž 0 0 0 0 R2 R12 NPN Hybrid Sensors - open collector NPN output 000 000 C11 - USER - C10 TTL - open collector NPN output Q2 TTL - standard Totem-pole output Ó 0 **O** – R17 – **O** Щ Q1 **Basic Variable Reluctance** ĒD 0 - R16 - 0 (O O) 0 R4 – O AC derived from a Transformer Winding Ē 0 R5 - 0 SIGNAL **O** – R15 – **O** 0 - R9 -0 C14 O 0-See over page for detailed connection scenarios for each of the above signal sources. **O** – R14 – **O** IC1 ΥR 0-R11 – **O** ū 000 0000000 POWER Q D3 0 LED2 3 R8 0 **O**^{*} 00 OUT 0000000 0 0 R10 - O Bottom two Terminals are Signal out; $V_{(out)} = +5V$ Full Scale. Measure using a device with $Z_{(in)} > 10k$. RANGE FILTER(1) **00** C 3 00 С USER USER в **ОО** _D BOOD 0 Ò Ò Ò 0 Q ò ò ò ò 0 ò C3 C5 C2 Making it work in 3 steps Not shown actual size

Step 1 ~ Fix the Input Frequency Range

From a knowledge of the signal source, determine the maximum source frequency, f(in)(max). Look at the graph - Input Frequency related to Range Capacitance, and find f(in)(max) on the x-axis. Trace up to both data-lines and across to the y-axis. Read off the Range Capacitance from anywhere between the two y-axis intercepts.

Example 1 - find f_{(in)(max)} = 70kHz on the x-axis. Trace up to both data-lines and across to the y-axis. Read off the Range Capacitance from anywhere between the two y-axis intercepts; the only possible value here is 120pF. This capacitor is pre-installed; select with JP1 in position A-C. Step 1 complete

Example 2 - find f(in)(max) = 1kHz on the x-axis. Trace up to both data-lines and across to the y-axis. Read off the Range Capacitance from anywhere between the two y-axis intercepts; a good choice here is 4700pF. This capacitor is pre-installed; select with JP1 in position A-B. Step 1 complete.

Example 3 - find f_{(in)(max)} = 80Hz on the x-axis. Trace up to both data-lines and across to the y-axis. Read off the Range Capacitance from anywhere between the two y-axis intercepts; a good choice here is 68nF. Solder this capacitor (see note 7) into position C12; select with JP1 in position C-D. Step 1 complete

Step 2 ~ Fix the Filtering

The value of $f_{(in)(max)}$ will be known from step one above. This same value is now used to determine the minimum Filter capacitance needed to keep Output Voltage Ripple at or below 5% or 250mV_(pk-pk) (see note 5). Look at the graph - Input Frequency related to Filter Capacitance (see note 6). Find $f_{(in)(max)}$ on the x-axis. Trace up to the data-line and across to both y-axes. From the primary y-axis, read off the minimum Filter capacitance. From the secondary y-axis, read off the Output Voltage Rise and Fall Times (see notes 3 & 4).

If the indicated minimum Filter capacitance does not fall on a preferred value, choose the next larger value. The absolute minimum Filter capacitance is set at 2200pF (installed), so all values of $f_{(in)(max)}$ above 12kHz will always have <5% Output Voltage Ripple, and Output Voltage Rise/Fall Times of 250us (0.25ms). Note, there is no maximum value of Filter capacitance, it may be increased without bound.

Example 1 - find f(in)(max) = 12kHz on the x-axis. Trace up to the data-line and across to both y-axes. From the primary y-axis, read off the Filter on A-C his capacitor is pre-in alled (C5): select with JP2 From t



Input Frequency related to Filter Capacitance



Output Voltage Rise and Fall Times - 220us or 0.22ms. Step 2 complete.

Example 2 - find f(in)(max) = 500Hz on the x-axis. Trace up to the data-line and across to both y-axes. From the primary y-axis, read off the Filter capacitance - 220,000pF, 220nF or 0.22uF. Solder this capacitor (see note 7) into position C13, and select with JP2 in to position C-D. From the secondary y-axis, read off the Output Voltage Rise and Fall Times - 22,000us or 22ms. Step 2 complete.

Example 3 - find f(in)(max) = 110Hz on the x-axis. Trace up to the data-line and across to both y-axes. From the primary y-axis, read off the Filter capacitance - 1uF. This capacitor is pre-installed (C4); select with JP2 in position A-B. From the secondary y-axis, read off the Output Voltage Rise and Fall Times - 100,000us, 100ms or 0.1sec. Step 2 complete.

Step 3 ~ Connect-up

Continue over page and make all electrical connections. When powered, use the Adjust Full Scale potentiometer to fine tune the Output Voltage.

Note 1: FSR_(min) is $f_{(in)}$ with Adjust Full Scale potentiometer set fully clockwise & $V_{(out)} = 5V$. Note 2: $FSR_{(max)}$ is $f_{(in)}$ with Adjust Full Scale potentiometer set fully anti-clockwise & $V_{(out)} = 5V$. Note 3: Rise & Fall Times are 10% to 90% & 90% to 10% respectively of $V_{(out)}$ when $V_{(out)(max)} = 5V$. Note 4: Rise & Fall Times are measured using $f_{(in)}$ = 70kHz with 100% A.M. at $f_{(in)}$ / 1000 with a 1:1 M/S ratio. Note 5: Output Ripple Voltage is measured pk-pk & Steady-State (no modulation). Note 6: This graph shows values of $f_{(in)(max)}$ when $V_{(out)(ripple)} = 5\%$ of $V_{(out)(ave)}$ (250mV pk-pk), and $V_{(out)(ave)} = 5V$. Note 7: Choose capacitors from FEC/Wima Polypropylene FKP2 series, or second choice from FEC/Wima Polyester MKS2 series.



General Description (Continued)

This circuit is made up of three functional sections - input signal conditioning, followed by signal conversion, and ending with signal filtering and the output driver. The front-end (FE) signal conditioning copes with signals from a variety of sources, the six most common of which are detailed below. The signal converter is designed around the LM2907N, which is a frequency-doubling charge-pump device. The Full Scale Input frequency is simply set using just one capacitor (see Step 1 on front of leaf), and the degree of Signal Filtering is also accomplished with just one capacitor (see Step 2 on front of leaf). The output driver is an emitter follower, producing <15mV of output offset for an input frequency of zero Hertz. Linearity is excellent at better than +/-1%, and the whole circuit consumes less than 20mA.

In setting-up the on-circuit filter, one must remember that Output Voltage Response times are inextricably linked to Output Voltage Ripple. To be precise, increasing Filter capacitance reduces ripple voltage but increases response times. For most engineers then, there is a minor dilemma - rapid Output Voltage Response times cannot be achieved without some degree of Output Voltage Ripple.

For example, it is impossible to arrange Output Voltage Response times of 5ms for an input frequency of 50Hz. This is because a frequency of 50Hz has a period of 20ms, which is longer than the desired rise and fall times of 5ms. The output voltage will, therefore, be all-but unfiltered, rising and falling between 0V and +5V in delayed sympathy with the input signal. To avoid this problem, a graph is presented (front of leaf) linking these four variables - 'Filter Capacitance', 'Full Range Input Frequency', 'Output Voltage Ripple (at 5%)', and 'Output Voltage Response Time'.

From the graph, it is easy to determine both the smallest acceptable amount of Filter capacitance, and the resulting Output Voltage rise and fall (response) times. Note - the smallest acceptable amount of Filter capacitance is defined here as - the smallest value of Filter capacitance that will keep the Output Voltage Ripple at, or less than, 5% (250mV_(pk-pk)) of the full scale output voltage (5Volts) for a particular Full Scale Input Frequency. As a result, the supplied graph delivers a Filter capacitance that optimises the two Output Voltage variables of Ripple and Response time. Note however, there is effectively no upper limit to the amount of Filter capacitance, it can be increased without bound to reduce Output Voltage Ripple.



IMPORTANT

Every care has been exercised in the design of this product. It has been designed and constructed with electrical robustness and reliability in mind. However, incorrect connection to power sources, signal sources and measuring devices may stress the circuit to the point of damage. Always double-check before powering this circuit and other connected devices. All circuit boards are 100% tested.

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